IN THE CLAIMS:

Please amend Claim 1 as shown below. The claims, as pending in the subject application, now read as follows:

1. (Currently amended) A processor system on a single semiconductor substrate, wherein the processor system is provided with a built-in processor, a memory controller, an external bus interface that can connect an external processor from outside of a single semiconductor substrate, a processor bus which is connected with the built-in processor and the external bus interface, and a connection unit that mutually connects the memory controller and the processor bus,

wherein first and second signal lines for inputting first and second enable signals are connected to reset signal lines of the built-in processor and the external bus interface, respectively ~~are responsive to respective enable signals~~,

and wherein one of the first and second ~~respective~~ enable signals is asserted while the other one of the ~~respective~~ first and second enable signals is deasserted, so that one of the built-in processor and the external bus interface ~~corresponding~~ to which the asserted enable signal is input can be in a reset state and the other one of the built-in processor and the external bus interface can use the processor bus ~~be used~~ exclusively.

2. (Original) The processor system according to claim 1, wherein the connection unit includes a crossbar switch.

3. (Original) The processor system according to claim 1, wherein the connection unit includes a common bus.

4. (Original) The processor system according to claim 1, further comprising:

a second built-in processor connected to the connection unit on the semiconductor substrate.

5. and 6. (Cancelled)

7. (Original) The processor system according to claim 1, wherein the built-in processor and the external bus interface are connected through a bus common to the connection unit.

8. (Previously Presented) The processor system according to claim1, wherein the built-in processor and the external processor use in common programs stored in a memory controlled by the memory controller.

9. (Original) The processor system according to claim 1, further comprising:

an image data transfer bus connected with the connection unit; and

an image output device interface or an image input device interface connected with the image data transfer bus on the semiconductor substrate.